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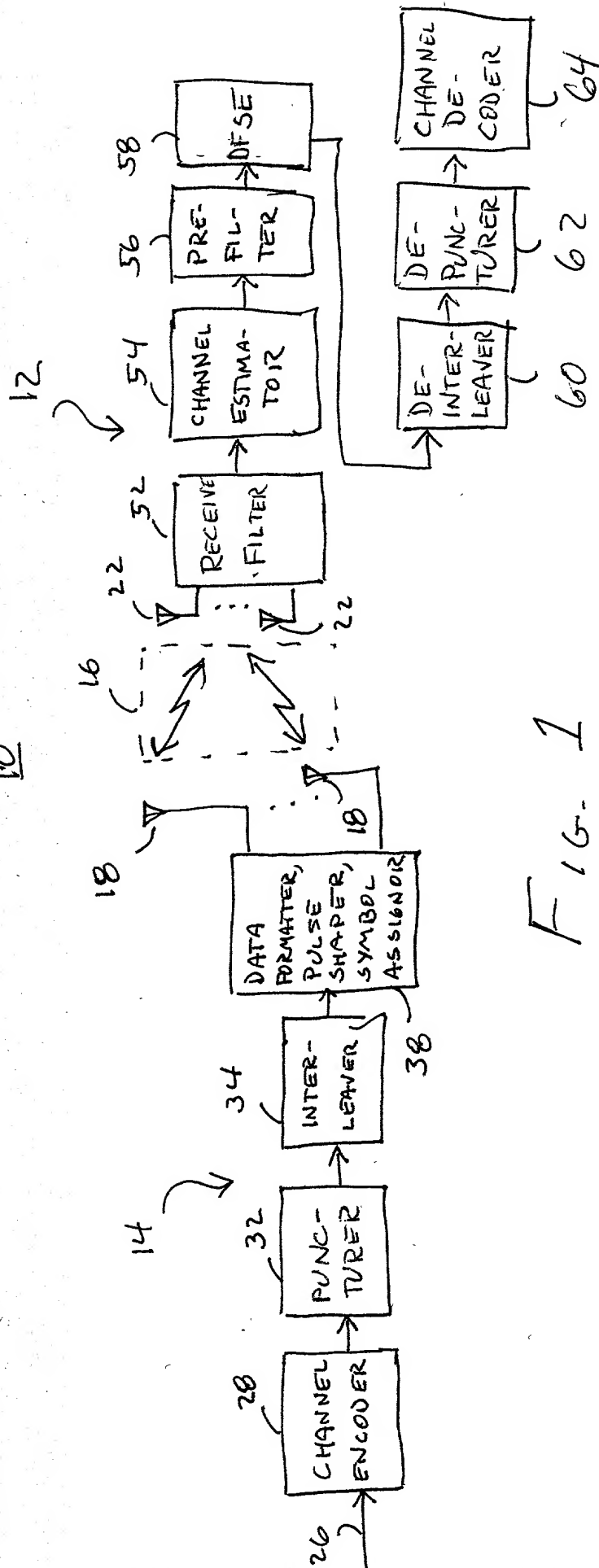


Fig. 1

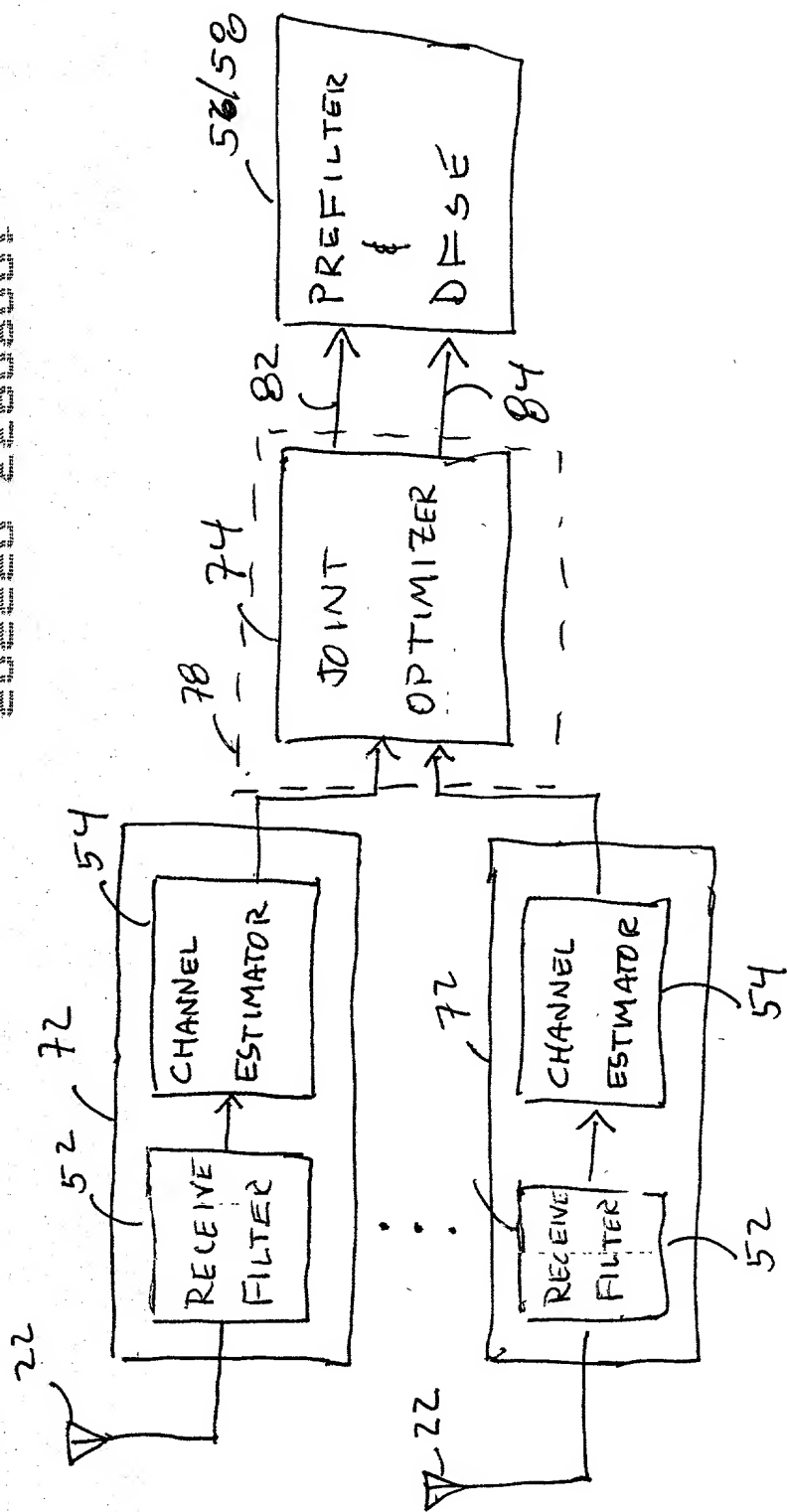


Fig. 2

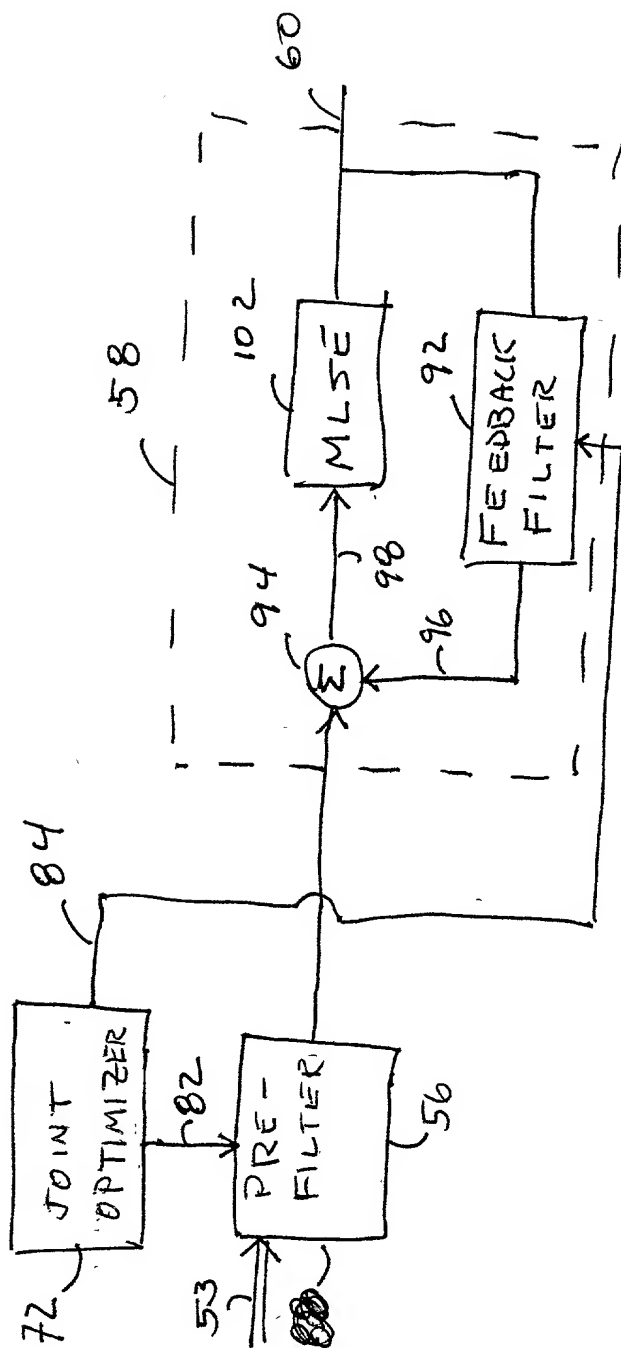


FIG. 3

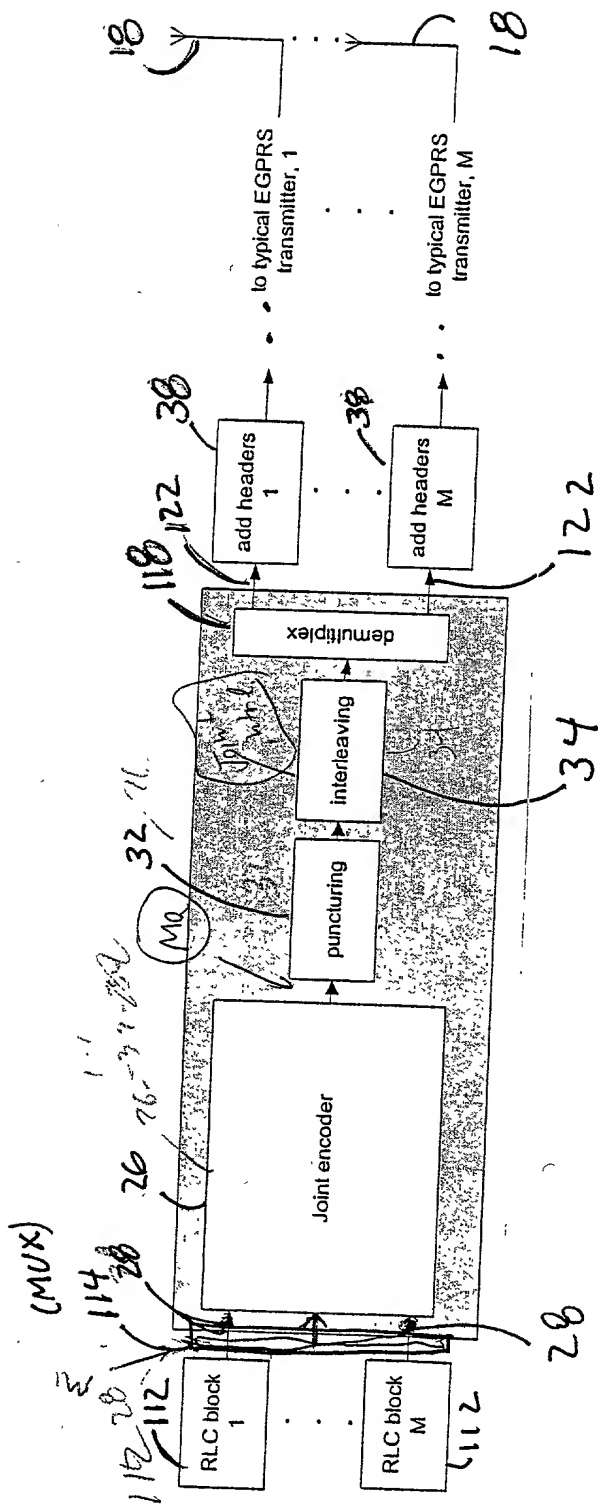


FIG. 4

FIG. 5 is a block diagram of a receiver system. The system includes two parallel processing paths. Each path starts with a Receive Filter (122) receiving an input signal (22). The outputs of the Receive Filters (122) are fed into a Joint Channel estimator (124). The Joint Channel estimator (124) outputs channel estimates (126) to two Space-Time Prefilters (126). Each Space-Time Prefilter (126) outputs to a SISO Equalizer (128). The outputs of the SISO Equalizers (128) are fed into a Multiplex block (132). The Multiplex block (132) outputs to a Joint Turbo Decoder (134). The Joint Turbo Decoder (134) outputs to a Remove tail bits block (136). The Remove tail bits block (136) outputs to a De-Multiplex block (142). The De-Multiplex block (142) outputs two parallel streams of 462 bits each (144).

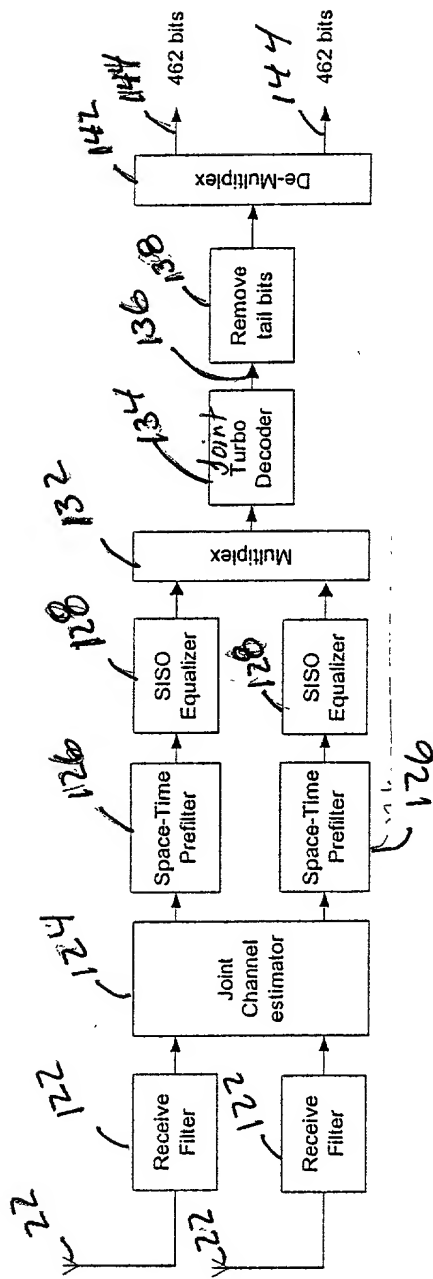


FIG. 5

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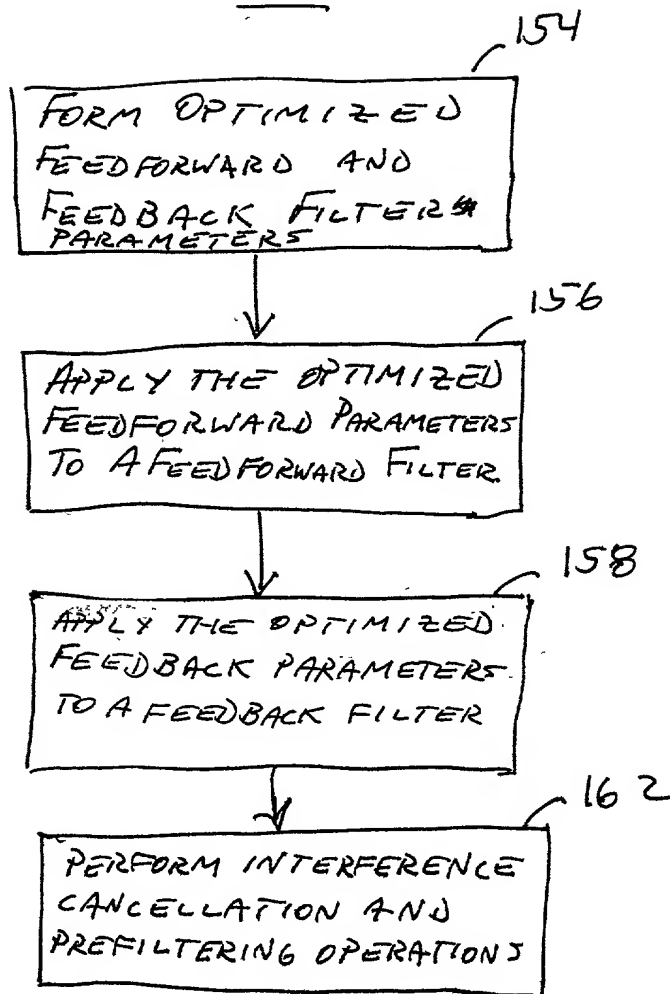


FIG. 6